



Form PTO-1449 (Modified)				Atty Docket No.:	Serial No.:			
				03692.P054D2	10/647,925			
List of Patents and Publications Statement (Use several sheets if necessary)				Applicants:				
				Disney, D.				
				Filing Date: August 26,2003				
REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS					
Exam. Initial		Date	Document Number	Name		Class	Sub-Class	Filing Date
FOREIGN PATENT DOCUMENTS								
No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
Loke		JP 6-224426	08/12/94	Japan	Uno			English
Loke		DE 43 09 764	09/29/94	Germany	Tihanyi, et al.			
Loke		JP 56-38867	04/14/81	Japan	Okabe, T., et al.			English
Loke		JP 57-10975	01/20/82	Japan	Sanyo			English
Loke		JP 57-12557	01/22/82	Japan	Tanaka, et al.			English
Loke		JP 57-12558	01/22/82	Japan	Tanaka, et al.			English
Loke		JP 60-64471	04/13/85	Japan	Saitou, M.			
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)								
Loke		"International Electron Devices Meeting 1979- Washington, D.C, Dec. 3-4-5," Sponsored by Electron Devices Society of IEEE, Pages 238-241.						
Loke		"Realization of High Breakdown of Voltage (>700V) in Thin SOI Devices," S. Merchant, et al., Phillips Laboratories North America, 1991 IEEE, Pages 31-35.						
Loke		"Theory of Semiconductor Superjunction Devices," T. Fujuhana, Japanese Journal of Applied Physics, Part 1, October 1997, Vol. 36, No. 10, Pages 6254-6262.						
Examiner			Date Considered					
Loke			6/29/04					
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.								



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Form PTO-1449 (Modified) TRADEMARK OFFICE				Atty Docket No.:	Serial No.:			
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FOREIGN PATENT DOCUMENTS								
No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
Loke		JP 3-211771	09/17/91	Japan	Toshiba			English
Loke		JP 4-1078677	04/09/92	Japan	Yamanishi, et al.			English
Loke		JP 57-12558	01/22/82	Japan	Tanaka, et al.			English
Loke		WO 99/34449	07/08/99	PCT	Letavic, et al.			
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)								
Loke		"Air-Gap Formation During IMD Deposition to Lower Interconnect Capacitance," B. Shieh, et al., IEEE Electron Device Letters, Vol. 19, No. 1, January 1998.						
Loke		"Oxide-Bypassed VDMOS (OBVDMOS): An Alternative to Superjunction High-Voltage MOS Power Devices," Yung C. Liang, et al., IEEE Electron Device Letters, Vol. 22, No. 8, August 8, 2001, Pages 407-409.						
Loke		"Comparison of High-Voltage Devices for Power Integrated Circuits," R. Jayaraman, et al., IEDM 84, 1984, Pages 258-261.						
Loke		"A New Generation of High-Voltage MOSFETs Breaks the Limit Line of Silicon," G. Debby, et al., Siemens AG, Munchen, Germany, IEDM 98-683 – IEDM 98-685.						
Examiner				Date Considered				
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)								
<i>Loke</i>		"High Performance 600 V Smart Power Technology Based on Thin Layer Silicon-on-Insulator," T. Letavic, et al., Phillips Electronics North America Corp., 4 Pages.						
<i>Loke</i>		"Modern Semiconductor Device Physics," S. M. Sze, John Wiley & Sons, 1998, Chapter 4, Pages 203-206.						
<i>Loke</i>		"Modeling Optimization of Lateral High Voltage IC Devices to Minimize 3-D Effects," H. Yilmaz, R&D Engineering, GE Corp., NC, Pages 290-297.						
Examiner <i>Loke</i>			Date Considered <i>6/29/04</i>					
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